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Final Report
High-Electron Mobility Graphene Channel Transistors for Millimeter-Wave Applications

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***Abstract*—We have fabricated and characterized the graphene-channel field effect transistors (GFETs) on semi-insulating SiC substrates. In our first GFETs, the device exhibits n-type FET operation with the transconductance of 0.1 mS/mm at the drain voltage of 0.5 V. The current gain cutoff frequency characterized by S parameter measurement is 0.5 GHz. These characteristics are primarily limited by the low carrier mobility of 50 cm^2/V.s. evaluated by Hall measurement. Further improvement in the graphene quality and the process technique to avoid the damage on graphene channel will be the key targets of the study in the next year.**

I. INTRODUCTION

Graphene – a single layer of graphite – has been paid much attention as its unique electron property. Ideal graphene is able to realize the mass-less electrons because of the Dirac-corn-shaped band profile [1,2]. From a practical point of view, such a perfect mono-layer graphene is not the only target of interest. A few layer graphene (FLG) exhibits more semiconductor-like property with small bandgap and large electron mobility. Reported electron mobility is as much as that of InAs. In addition, the existence of bandgap opening is predicted for the epitaxial graphene on SiC substrates due to the graphene-substrate interaction [3]. Therefore FLG could be a promising candidate for millimeter- and submillimeter-wave ultra-high frequency applications in which currently narrow-bandgap III-V semiconductors (e.g., antimonide) are the primary technology of interest.

To realize integrated circuits by the FLG-channel transistors, top-down lithography process is mandatory. From this viewpoint, epitaxial FLG, produced by a thermal decomposition of SiC [1] is more suitable than the exfoliated FLG [2]. In addition, epitaxial FLG on semi-insulating SiC substrates has an advantage in the high-frequency operation.

In this study, we will study the growth of FLG and apply this FLG to the transistor fabrication. The FLG is grown on semi-insulating SiC substrates by the annealing in ultra-high vacuum. The surface treatment and the formation of the gate stack are important step to fabricate transistors. We will also study these by using the chemical vapor deposition system. The goal of this research is to achieve high electron mobility of over 10,000 cm^2/Vs by epitaxial FLG at room temperature and to obtain the transistor operation of top gate FLG-channel transistors and characterize their high-frequency performance by means of S parameter measurements.

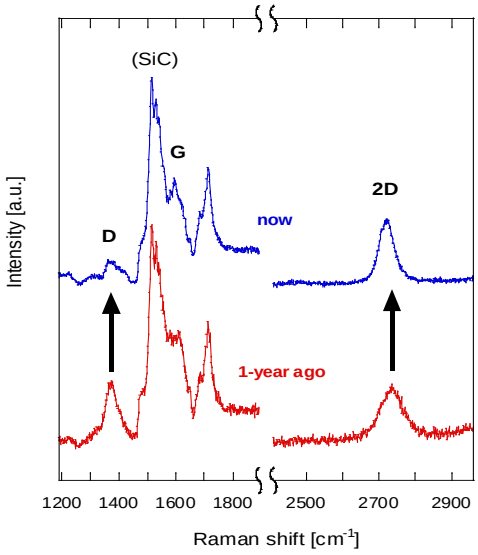

Figure 1. Raman-scattering spectra of graphene on semi-insulating SiC grown recently (now) and at the first time in this project (1-year ago).

II. FORMATION OF EPITAXIAL GRAPHENE

For the growth of FLG, we use a gas source molecular beam epitaxy (GS-MBE) reactor that is originally used to grow SiC layer on Si substrates. This enables us to anneal the substrate in ultra-high vacuum condition. Indeed we have confirmed the formation of FLG at the surface of SiC grown on Si substrates [4]. Similar approach will be possible for semi-insulating 6H- or 4H-SiC substrates. We will use these

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14. ABSTRACT

Graphene-channel field effect transistors (GFETs) on semi-insulating SiC substrates were fabricated and characterized. In the first GFETs, the device exhibits n-type FET operation with the transconductance of 0.1 mS/mm at the drain voltage of 0.5 V. The current gain cutoff frequency characterized by S parameter measurement is 0.5 GHz. These characteristics are primarily limited by the low carrier mobility of 50 cm2/V.s. evaluated by Hall measurement. Further improvement in the graphene quality and the process technique to avoid the damage on graphene channel will be the key targets of the study in the next year.

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substrates in this study because they are more suitable for high frequency applications than conductive Si substrates. The growth temperature and time are optimized to achieve high carrier mobility at room temperature. The quality of graphene has been improved as shown in the Raman spectra in Fig. 1. Comparing to the material grown one year ago, recently-grown graphene has smaller D band peak, indicating less defect in the material. In addition, 2D band peak becomes sharper and the peak shifts to lower wave number. This suggests that the recent graphene has better uniformity with respect to the number of graphene layers. Hall effect measurement at room temperature reveals the electron mobility of 50 cm^2/V.s and the sheet carrier concentration of 1 x 10^{13} cm^{-2}.

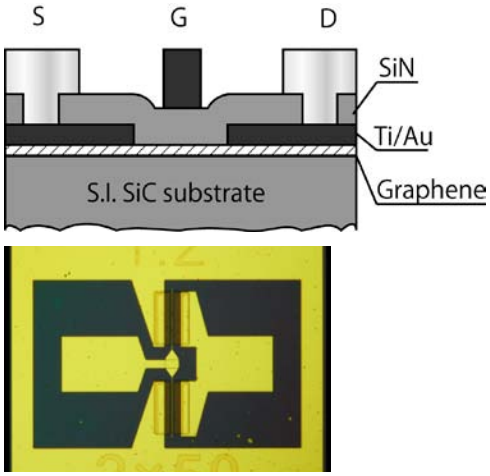

Figure 2. (top) Cross section of graphene-channel FET. Gate length is 0.5 μm. (bottom) Microscope image of top-gate FET with coplanar probing pad.

III. Fabrication Process of GFET

The fabrication of graphene-channel field-effect transistors (GFETs) starts with Ti/Au lift off for the ohmic electrodes. The graphene channel is then defined by oxygen plasma etching. As the gate stack, a 50-nm-thick SiN is deposited by plasma-enhanced chemical vapor deposition (PECVD). The gate metallization is done by e-beam lithography and the lift off of Ti/Au. The gate length is 0.5 μm. After opening the contact holes for the ohmic electrodes, Ti/Au is lifted off for probing pad. The cross section and top view of an FET are shown in Fig. 2.

In the ohmic metallization, the surface cleaning plays one of the key roles on the contact resistance and the adhesion of the electrode. Usually in the semiconductor process the oxygen plasma ashing is commonly used to get rid of the resist scum remaining after the lithography process. However in the graphene process the oxygen plasma cannot be applied in this purpose because it etches the graphene channel. As an alternative method, we used the hydrogen treatment. After the lithography step, the sample is annealed for 2 hours at a pressure of 100 Pa with flowing the mixture of hydrogen and nitrogen (H_2:N_2 = 1:1). The temperature is fixed at 100°C in order to avoid the degradation in the resist pattern. The AFM images of the sample surface before and after the hydrogen treatment are shown in the Fig. 3. The atomic layer steps hidden by the resist scum are able to be observed after the hydrogen treatment. We confirmed a significant improvement in the adhesion of ohmic metal by introducing this hydrogen treatment process.

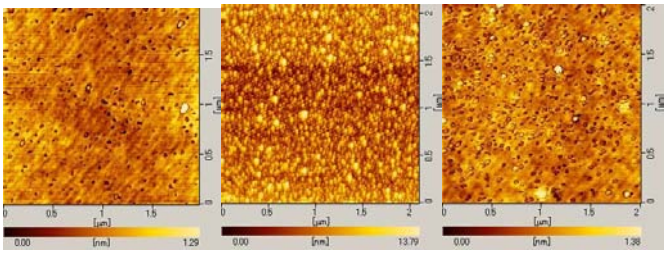

Figure 3. Change in surface morphology by lithography process: (a) as grown surface of graphenized SiC substrate, (b) after resist strip, and (c) after hydrogen cleaning at 100°C.

As the gate stack, we tested SiO_2 and SiN by PECVD. However, when we deposited SiO_2 on graphene, the peaks associated with the graphene were disappeared in Raman spectra. On the other hand, the PECVD of SiN preserves the graphene-related peaks in Raman spectra. This result suggests that the PECVD process of SiO_2 causes a serious damage on graphene, possibly due to the oxygen plasma since the oxygen was introduced only for SiO_2.

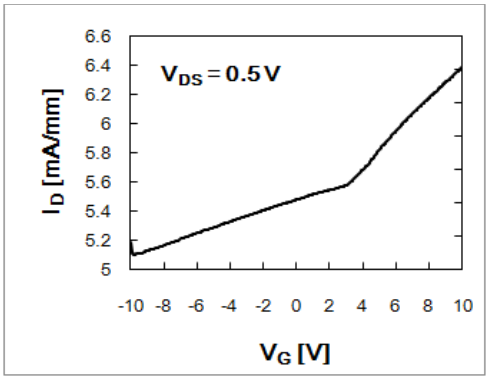

Figure 4. I_D-V_G characteristics of graphene FET on 6H-SiC substrate.

IV. Results and Discussion

Figures 4 show typical drain current (I_D)-gate voltage (V_G) characteristics of graphene FETs on a SiC substrate. This exhibits the n-type FET behavior at all range of V_G tested.

The peak transconductance is 0.1 mS/mm at the drain-to-source voltage (V_{ds}) of 0.5 V. High-frequency performance is characterized by the S parameters measured by a vector network analyzer with Cascade coplanar microprobes. The pad parasitics are de-embedded using the open and short dummy devices. The resulting current gain is shown in Fig. 5 from which the current gain cutoff frequency (f_T) is 0.5 GHz for the GFET on the SiC substrate. The small signal equivalent circuit parameters are extracted from the measured S parameters at the maximum f_T. The source resistance (R_s) and drain resistance (R_d) are both 10 Ω.mm. The gate-source capacitance (C_{gs}) and the gate-drain capacitance (C_{gd}) are 250 fF/mm and 200 fF/mm, respectively. Comparing to the conventional III-V high-frequency FETs, the R_s and R_d are quite large by one order of magnitude. This large parasitic resistance is primarily due to the low mobility and resulting large sheet resistance of the graphene channel (12k Ω/sq). For further improvement in the carrier mobility, we are paying more attention to the surface morphology of SiC substrates.

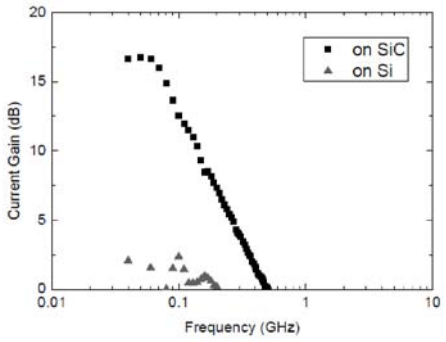

Figure 5. Frequency dependence of current gain obtained by S-parameter measurement. Current gain cutoff frequency (f_T) is 0.5 GHz for device on SiC substrate, and less than 0.2 GHz for device on Si substrate. V_G = 3 V and V_D = 10 V.

V. CONCLUSION

Graphene-channel field-effect transistors on semi-insulating SiC substrates are fabricated and characterized. In the FET process, the hydrogen treatment is adapted for the lift-off process in the ohmic contact on graphene. For the gate stack, SiN is found to be more appropriate than SiO_2 to avoid the damage on graphene due to oxygen plasma. The first FET exhibits the tranconductance of 0.1 mS/mm, and the current gain cutoff frequency of 0.5 GHz. These characteristics are primarily limited by the low carrier mobility of 50 cm^2/V.s. evaluated by Hall measurement. Further improvement in the graphene quality and the process technique to avoid the damage on graphene channel will be the key targets of the study in the next year.

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